REMARKS

Claims 1-98 are pending, with claims 17-50 and 67-98 withdrawn from consideration.

Claim 12 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant believes the Examiner intended to reject claim 14 rather than claim 12, because "the computing element" is recited in line 3 of claim 14 rather than claim 12. The amendment to claim 14 is believed to overcome this rejection. Also, claims 64 and 66 have been amended to correct minor informalities.

Claims 1-16 and 51-66 remain rejected under 35 U.S.C. § 102(e) as being anticipated by Sharrit et al. (U.S. Patent No. 5, 999,990).

Claims 1-16 are directed to a processor having a plurality of kernel planes with a plurality of kernels for processing data in a communication device. At least one kernel of the plurality of kernels has an interface adapted to receive and transmit information from the at least one kernel, a satellite kernel coupled to the interface, the satellite kernel performing a discrete class of operations within a communications application, and a local controller coupled to the interface and the satellite kernel and permitting the satellite kernel to operate autonomously with respect to the other of the plurality of kernels in the respective kernel plane. Claims 51-66 are directed to a computer readable medium containing therein computer readable codes that enable an electronic device to access the at least one kernel.

Sharrit et al. is directed to a communicator 10, which includes a plurality of reconfigurable resource units (RRUs) 13, a signal bus 14, a controller 16, etc. The plurality of RRUs 12 can each be dynamically altered to perform any of a plurality of processing tasks. The controller 16 determines a plurality of processing tasks to be supported by the communicator and configures the plurality of RRUs 12 accordingly.

As illustrated in Fig. 3 of Sharrit, an RRU 54 can include a general purpose processor (GPP) 48 and a field programmable gate array (FPGA) 50. To configure the FPGA 50, the GPP 48

delivers a configuration file to an input of the FPGA 50. The GPP 48 is coupled to the controller 16 for receiving instructions on how to process a signal on bus 14. In response to the instructions, the GPP 48 delivers a control signal to FPGA 50 instructing it to read the signal on signal bus 14 and to process the signal in an appropriate area of the cell array.

Alternatively, as illustrated in Fig. 4 of Sharrit, an RRU 58 can include both hardware and software programmability. That is, RRU 58 includes a GPP 60, an FPGA 62, a DSP 64 with associated RAM 66, and a multiplexer 68. RRU 58 is a hybrid unit which allows controller 16 to specify whether a signal currently on signal bus 14 will be processed in hardware (in FPGA 62) or in software (in DSP 64). Based on commands from controller 16, GPP 60 delivers a select signal to multiplexer 68 that directs the signal on bus 14 to the desired processing unit. Also, as indicated by the arrows, the GPP 60 configures the FPGA 62 or the DSP 64 to run certain software modules.

Sharrit does not teach, or even suggest, a kernel having a local controller that permits the kernel to operate autonomously with respect to other of a plurality of kernels, as required by the claimed invention. Sharrit has centralized control in its controller 16 as opposed to the claimed distributed control. Sharrit's controller 16 MIPS rating and bus 14 width and speed ratings limit the number of RRU's or the reconfiguration abilities versus time. With equal ratings for the controller and buses, the distributed control system of the claimed invention is more scaleable in that it can support more kernels or more reconfigurations per second than Sharrit.

Contrary to the Examiner's statement on page 3 of the Office Action, Sharrit's GPP (general purpose computer), which operates in conjunction with a FPGA (Fig. 3) or a FPGA and DSP (Fig. 4), is not equivalent to the claimed local controller. There is no suggestion in Sharrit that the GPP performs local controller functions. All control must be centralized in the controller 16. In order for the GPP to perform local controller functions and do resource allocation, it would need to obtain information from the DSP and/or FPGA. Since information is transmitted only from the GPP to the DSP and/or the FPGA and not the reverse (as indicated by the single-headed arrow), the GPP can not know how loaded the DSP is. Only through the local controller 16 can the GPP know this information.

Further, the Sharrit system does not scale well as the number of RRU increases. The performance of the single controller 16 and bus 14 places a limit on the maximum number of RRUs. For example, assume Sharrit has one chip with 4 RRUs and another chip with 8 RRUs. If Sharrit then requires a chip with 16 RRUs, the single controller 16 and bus 14 must be redesigned for higher performance (which may not even be possible). Thus Sharrit does not have good scalability.

On the other hand, the claimed kernel's local controller scales wells as the number of kernels increases. In a system with distributed control, the performance of the local controllers in the respective kernels do not increase as a function of total kernels. That is, the individual kernels do not increase in complexity as the network grows. All kernels simply run the same protocol, and as the network grows kernels may experience longer latencies. If the application can tolerate increased or unknown latency, then the local controllers may not need to increase in complexity. By way of analogy, a computer connected to an IP network does not require the individual computers to increase in complexity and performance as the number of networked computers increases.

In view of the above remarks, it is respectfully submitted that claims 1-16 and 51-66 are patentable over Sharrit. Reconsideration and withdrawal of this rejection is therefore respectfully requested.

Finally, the Examiner states in paragraph 24 of the Office Action that "Applicant's arguments with respect to claims 1-16 and 51-66 have been considered but are moot in view of the new ground(s) of rejection." This statement is not clear in the context of the Office Action because the Examiner has maintained the prior art rejection.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By Laura C. Brutman

Laura C. Brutman
Registration No.: 38,395
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 753-6237 (Fax)
Attorneys/Agents For Applicant